AMENDMENTS TO THE CLAIMS

1. (Cancelled)

2. (Currently Amended) The power up reset circuit of claim [[1]] 4, wherein the at least one diode connected transistor coupled to the first input tries to maintain a one or more threshold voltage (Vt) difference from the power supply voltage at the first input.

3. (Currently Amended) The power up reset circuit of claim [[1]] 4, wherein the at least one diode connected transistor or the at least one resistor divider coupled to the second input tries to maintain a one or more threshold voltage (Vt) difference from ground potential.

4. (Currently Amended) ~~The power up reset circuit of claim 1, wherein a first plurality of diode connected transistors are coupled in series and coupled to the first input of the comparator~~ A power up reset circuit, comprising:
a comparator having first and second inputs and an output;
a plurality of first diode connected transistors connected in series between the first input and a power supply voltage;
a first resistor connected between the first input and ground potential;
at least one second diode connected transistor or at least one resistor divider coupled between the second input and ground potential; and
a reset signal generated at the output when the voltages at the first and second inputs are approximately the same.

5. (Currently Amended) The power up reset circuit of claim 4, wherein a ~~second~~ plurality of second diode connected transistors are coupled ~~in series and coupled to~~ between the second input of the comparator and ground potential.

6. (Currently Amended) The power up reset circuit of claim [[1]] 4, further comprising:
a hysteresis circuit coupled to the comparator, the hysteresis circuit configured

to protect the power up reset circuit from glitches in the power supply voltage or the ground.

7. (Original) The power up reset circuit of claim 4, wherein the hysteresis circuit is further configured to lower a voltage level that the power supply voltage provides to the power up reset circuit in order to cause a change in the reset signal.

8. (Cancelled)

9. (Currently Amended) The integrated circuit of claim [[8]] 12, wherein the integrated circuit comprises a Field Programmable Gate Array (FPGA).

10. (Currently Amended) The integrated circuit of claim [[8]] 12, wherein the comparator provides a two state output signal at the output, a first or high logic level output state or a second or low logic level output state.

11. (Currently Amended) The integrated circuit of claim [[8]] 12, wherein the first diode connected transistor is connected directly to ground.

12. (Currently Amended) ~~The integrated circuit of claim 8~~ An integrated circuit having a power up reset circuit, comprising:
a power supply directly connected to a first resistor, the first resistor in series with a first input node and a first diode connected transistor, the first diode connected transistor connected to ground;
a second diode connected transistor directly connected to the power supply and connected in series with a second input node and a second resistor, wherein the second resistor is directly connected to ground; and
a comparator connected to the first input node and second input node and producing a reset signal when the voltages at the first and second input nodes are about equal, wherein the reset signal is at an output node between a first capacitor connected to the power supply and a second capacitor connected to ground.

13. (Currently Amended) ~~The integrated circuit of claim 8~~ An integrated circuit having a power up reset circuit, comprising:
a power supply directly connected to a first resistor, the first resistor in series with a first input node and a first diode connected transistor, the first diode connected transistor connected to ground;
a second diode connected transistor directly connected to the power supply and connected in series with a second input node and a second resistor, wherein the second resistor is directly connected to ground; and
a comparator connected to the first input node and second input node and producing a reset signal when the voltages at the first and second input nodes are about equal, further comprising a hysteresis circuit coupled to the comparator, the hysteresis circuit comprising a feedback transistor connected in parallel with a third resistor, wherein the gate of the feedback transistor is connected to the reset signal and wherein the third resistor is connected to the first diode connected transistor.

14-18 (Cancelled)

19. (New) The integrated circuit of claim 13, wherein the integrated circuit comprises a Field Programmable Gate Array (FPGA).

20. (New) The integrated circuit of claim 13, wherein the comparator provides a two state output signal at the output, a first or high logic level output state or a second or low logic level output state.

21. (New) The integrated circuit of claim 13, wherein the first diode connected transistor is connected directly to ground.